UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,855	12/02/2003	Steven L. Pline	10014281-1	3242

22879 7590 11/02/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
EHNE, CHARLES	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,855	PLINE ET AL.	
	Examiner	Art Unit	
	Charles Ehne	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8,10,11,13-17,23 and 26-35 are rejected under 35 U.S.C. 102(b) as being unpatentable by Hiratsuka (6,119,245).

As to claim 1, Hiratsuka discloses a data storage and retrieval system operating on a host computer, the data storage and retrieval system comprising:

a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the memory device, the sparing system comprising computer readable instructions stored in the host memory of the host computer (column 2, lines 31-41); and

an error correction code system configured to encode data with an error correction code, store the data into the memory device, and decode the encoded data with the error correction code to retrieve the data from the memory device, the error correction code system comprising computer readable instructions stored in the host memory of the host computer (column 5, lines 46-53).

As to claim 2, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table stored in the host memory (column 5, lines 54-57).

As to claim 3, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table stored in the memory device (Figure 15, column 7, lines 34-37).

As to claim 4, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table comprising entries obtained from a tester that tests the memory device (column 7, lines 16-67).

As to claim 5, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table comprising entries obtained from the sparing system that is configured to test the memory device to obtain the entries for the sparing table (column 7, lines 16-67).

As to claim 6, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table, and the sparing system and the error correction code system are configured to update the sparing table as defective memory sections are detected in the memory device (column 7, lines 46-53).

As to claim 7, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table and the error correction code system is configured to detect defective memory sections in the memory device, and the sparing system is configured to update the sparing table with address locations of

the detected defective memory sections in the memory device (column 5, lines 54-57 & column 7, lines 46-53).

As to claim 8, Hiratsuka discloses the data storage and retrieval system of claim 7, where the error correction code system is configured to correct errors in a selected memory section of the memory device, count the errors to obtain an error count and compare the error count to a threshold value to establish if the selected memory section is defective (column 7, lines 38-67).

As to claim 10, Hiratsuka discloses the data storage and retrieval system of claim 1, where the error correction code system is configured to encode and decode all data stored in the memory device (column 5, lines 46-53).

As to claim 12, Hiratsuka discloses the data storage and retrieval system of claim 1, where the error correction code system is configured to encode and decode selected data stored in the memory device (column 5, lines 46-53).

As to claim 13, Hiratsuka discloses a host computer, comprising:

a host host memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device (column 7, lines 38-53); and

a host processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer (column 7, lines 54-67).

As to claim 14, Hiratsuka discloses the host computer of claim 13, where the host processor executes instructions to replace addresses before the processor executes instructions to encode and decode data with the error correction code during data transfers (column 7, lines 16-30).

As to claim 15, Hiratsuka discloses the host computer of claim 13, where the host processor executes instructions to encode data with the error correction code before the processor executes instructions to replace addresses during a write operation (column 1, lines 51-61).

As to claim 16, Hiratsuka discloses the host computer of claim 13, where the processor executes instructions to provide sequential address data transfers between the storage device and the host computer (column 2, lines 31-41).

As to claim 17, Hiratsuka discloses the host computer of claim 16, where the sequential address data transfers are divided into sub-transfers around addresses of defective memory sections that are replaced with addresses of spare memory sections (column 2, lines 31-41).

As to claim 23, Hiratsuka discloses a computer system, comprising:

means for correcting errors in data retrieved from a storage style memory device, the means for correcting errors comprising computer readable instructions stored in a host memory of a host computer system (column 5, lines 46-53);

means for identifying defective sections of memory in the storage style memory device, where the defective sections of memory provide more errors than a predetermined threshold value (column 7, lines 54-67); and

means for sparing the defective sections of memory with replacement sections of memory in the storage style memory device, the means for sparing comprising computer readable instructions stored in the host memory of the host computer system (column 7, lines 63-66).

As to claim 26, Hiratsuka discloses the computer system of claim 23, where the means for identifying comprises:

means for counting the number of errors in a selected section of memory in the storage style device (columns 7-8, lines 67-3);

means for comparing the number of errors to the predetermined threshold value to obtain a compare result (column 8, lines 3-8); and

means for indicating if the selected section of memory is defective based on the compare result (column 8, lines 8-11).

As to claim 27, Hiratsuka discloses the computer system of claim 23, where the means for identifying comprises:

means for storing an address location of one of the defective sections (column 14, lines (column 8, lines 8-11); and

means for storing an address location of one of the replacement sections, where the address location of one of the replacement sections corresponds to the address location of one of the defective sections (column 7, lines 10-15).

As to claim 28, Hiratsuka discloses the computer system of claim 27, where the means for sparing comprises means for replacing the address location of one of the defective sections with the corresponding address location of one of the replacement

sections during data transfers between the computer system and the storage style memory device (column 7, lines 31-37).

As to claim 29, Hiratsuka discloses a method for storing and retrieving data, comprising:

providing a host computer and a memory device (column 5, lines 31-34);

providing computer-executable sparing instructions and error correction code instructions (column 6, lines 40-43);

replacing addresses for defective memory sections in a memory device with addresses for replacement memory sections in the memory device by executing the sparing instructions on the host computer (column 2, lines 31-41);

providing the addresses for the replacement memory sections to the memory device during read and write operations with the memory device by executing the error correction code instructions on the host computer (column 7, lines 31-37;

encoding original data with an error correction code to write encoded data into the memory device by executing the error correction code instructions on the host computer (column 5, lines 46-48); and

decoding data retrieved from a selected memory section of the memory device with the error correction code by executing the error correction code instructions on the host computer (column 5, lines 49-53).

As to claim 30, Hiratsuka discloses the method of claim 29, comprising:

maintaining a table of the addresses for defective memory sections and the addresses for replacement memory sections (column 5, lines 54-57 & column 7, lines 34-37); and

searching the table to match original addresses with the addresses for defective memory sections (column 7, lines 23-37).

As to claim 31, Hiratsuka discloses the method of claim 29, comprising:

updating a table with new addresses for defective memory sections (column7, lines 11-15); and

assigning new addresses for replacement memory sections that correspond with the new addresses for defective memory sections (column 7,lines 16-30).

As to claim 32, Hiratsuka discloses the method of claim 29, comprising:

counting errors in the data retrieved from the selected memory section to obtain an error count (columns 7-8, lines 67-3);

comparing the error count to error correction capabilities of the error correction code (column 8, lines 3-8); and

indicating the selected memory section is defective if the number of errors exceeds a predetermined portion of the error correction capabilities (column 8, lines 8-11).

As to claim 33, Hiratsuka discloses a method for storing and retrieving data, comprising:

providing a host computer and a storage style memory device (Figure 1.110 & column 6, lines 16-18);

providing computer-executable sparing instructions and error correction code instructions (column 7, lines 38-45);

sparing out sections of memory in the storage style memory device by executing the sparing instructions on the host computer (column 7, lines 54-67); and

encoding and decoding data stored in the storage style memory device with an error correction code by executing the error correction code instructions on the host computer (column 5, lines 46-53).

As to claim 34, Hiratsuka discloses the method of claim 33, comprising:

detecting grown defective sections of memory in the storage style memory device (column 7, lines 54-63); and

sparing out the detected grown defective sections of memory (column 7, lines 63-67).

As to claim 35, Hiratsuka discloses the method of claim 33, comprising:

encoding only selected data (column 5, lines 46-48); and

decoding only the encoded data stored in the storage style memory device (column 5, lines 49-53).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Martyn Riley (Non patent literature).

Hiratsuka discloses a data storage retrieval system operating on a host computer that provides a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the memory device (see claim rejection 1). Error correction code is used to encode and decode that data while the system stores and retrieves that data from the memory (see claim rejection 1). Hiratsuka fails to disclose wherein the error correction code is a Reed-Solomon error correction code.

Martyn Riley discloses an introduction to error correction codes with a wide range of applications in digital communications and storage (Page 1, lines 4-5). Martyn Riley does disclose wherein the error correction code is a Reed-Solomon error correction code (Page 1, lines 4-5)

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's error correction code with Martyn Riley's Reed-Solomon error correction code. A person of ordinary skill in the art would have been motivated to make the modification because Reed-Solomon codes can provide recovery for data that has encounter an error during transmission or while being stored (Martyn Riley: Page 1, lines 5-15).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Weng (5,428,630).

As to claim 9, Hiratsuka the data storage and retrieval system of claim 7, where the error correction code system is configured to correct errors in a selected memory section of the memory device, count the errors to obtain an error count and compare the error count to a threshold value to establish if the selected memory section is defective (see claim rejection 8). Hiratsuka fails to disclose wherein the threshold value is greater than 50% of a power of the error correction code.

Weng discloses a method and system for verifying the integrity of data written to a memory (Abstract, lines 1-2). The data is encoded and stored with error correction symbols in the memory and errors are detected when the decoder generates an error signal when the number of errors is greater than predetermined threshold number (Abstract, lines 8-19). Weng does disclose wherein the threshold value is greater than 50% of a power of the error correction code (column 8, lines 49-56 & column 9, lines 10-20)

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's threshold value with Weng's threshold value greater that 50% of a power of the correction code. A person of ordinary skill in the art would have been motivated to make the modification because a greater threshold allows for more data to be corrected and inturn less data is lost (Weng: column 9,lines 12-20).

Claims 18,19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Tsunoda (2003/0028733).

As to claim 18, Hiratsuka discloses a host computer, comprising: memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer (see claim 13 rejection). Hiratsuka fails to disclose wherein the host memory stores instructions for a digital camera and the processor executes the instructions to perform functions of the digital camera.

Tsunoda discloses an ECC control circuit in the memory interface control unit that checks whether an errors is present or not in data read from the memory, and corrects the data if an error is present. Tsunoda also discloses if a sector as a target for reading is a failed sector, an alternative sector control circuit detects an alternative

sector as a target for reading, and data is read from the detected alternative sector (Page 7, ¶ 0097, lines 11-18). Tsunoda does disclose wherein the memory stores instructions for a digital camera and the host processor executes the instructions to perform functions of the digital camera (Page 6, ¶ 0096, lines 16-19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's memory storing instructions with Tsunoda's memory that stores instructions for a digital camera. A person of ordinary skill in the art would have been motivated to make the modification because if a sector in the memory is bad the alternative sector control circuit will provide a alternative sector to read or write data to (Tsunoda: Page 7, ¶ 0097, lines 24-28)

As to claim 19, Hiratsuka discloses a host computer, comprising: memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer (see claim 13 rejection). Hiratsuka fails to disclose wherein the memory stores instructions for a personal digital assistant and the host processor executes the instructions to perform functions of the personal digital assistant.

Tsunoda discloses an ECC control circuit in the memory interface control unit that checks whether an errors is present or not in data read from the memory, and corrects the data if an error is present. Tsunoda also discloses if a sector as a target for reading is a failed sector, an alternative sector control circuit detects an alternative sector as a target for reading, and data is read from the detected alternative sector (Page 7, ¶ 0097, lines 11-18). Tsunoda does disclose wherein the memory stores instructions for a personal digital assistant and the host processor executes the instructions to perform functions of the personal digital assistant. (Page 6, ¶ 0096, lines 16-19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's memory storing instructions with Tsunoda's memory that stores instructions for a personal digital assistant. A person of ordinary skill in the art would have been motivated to make the modification because if a sector in the memory is bad the alternative sector control circuit will provide a alternative sector to read or write data to (Tsunoda: Page 7, ¶ 0097, lines 24-28)

As to claim 20, Hiratsuka discloses a host computer, comprising: memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers

between the storage device and the host computer (see claim 13 rejection). Hiratsuka fails to disclose wherein the storage device comprises a magnetic random access memory.

Tsunoda discloses an ECC control circuit in the memory interface control unit that checks whether an errors is present or not in data read from the memory, and corrects the data if an error is present. Tsunoda also discloses if a sector as a target for reading is a failed sector, an alternative sector control circuit detects an alternative sector as a target for reading, and data is read from the detected alternative sector (Page 7, ¶ 0097, lines 11-18). Tsunoda does disclose wherein the storage device comprises a magnetic random access memory (Page 10, ¶ 0124, lines 9-12).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Tsunoda's MRAM in place of Hiratsuka's flash memory. A person of ordinary skill in the art would have been motivated to make the modification because MRAM is also non-volatile, meaning it can be used to replace Flash and unlike Flash, MRAM does not degrade during writing, nor is it slower to write than to read.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Kleveland (2003/0115518).

As to claim 21, Hiratsuka discloses a host computer, comprising: memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a processor that executes the instructions to encode and decode data stored in the

storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer (see claim 13 rejection). Hiratsuka fails to disclose wherein the storage device comprises a phase change random access memory.

Kleveland discloses a memory device and method for redundancy and self repair (Abstract, lines 1-2). Kleveland does disclose wherein the storage device comprises a phase change random access memory (Page 7, ¶ 0053, lines 14-18).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Kleveland's phase change random access memory in place of Hiratsuka's flash memory. A person of ordinary skill in the art would have been motivated to make the modification because phase change random access memories are a well-known alternative (Kleveland: Page 7, ¶ 0053, lines 14-18).

As to claim 22, Hiratsuka discloses a host computer, comprising: memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers

between the storage device and the host computer (see claim 13 rejection). Hiratsuka fails to disclose wherein the storage device comprises a probe-based memory.

Kleveland discloses a memory device and method for redundancy and self repair (Abstract, lines 1-2). Kleveland does disclose wherein the storage device comprises a probe-based memory (Page 7, ¶ 0053, lines 14-18).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Kleveland's probe-based memory in place of Hiratsuka's flash memory. A person of ordinary skill in the art would have been motivated to make the modification because probe-based memories are a well-known alternative (Kleveland: Page 7, ¶ 0053, lines 14-18).

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Buternowsky (5,809,090).

As to claim 24, Hiratsuka discloses a data storage retrieval system that provides a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the memory device when the defective sections of the memory provide more errors than a predetermined threshold value (see claim rejection 23). Hiratsuka also discloses correcting errors in data retrieved from the memory device. Hiratsuka fails to disclose wherein the means for correcting errors comprises a multiple-bit per symbol error correction code.

Buternowsky discloses a communication system wherein response signals are in the form of digital packets, including forward error correction encoding and digital symbols that each consists of predetermined number of bits (Abstract, lines 3-5).

Buternowsky does disclose wherein the means for correcting errors comprises a multiple-bit per symbol error correction code (column 6, lines 23-24).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's error correction code with Buternowsky's multiple-bit per symbol ECCl. A person of ordinary skill in the art would have been motivated to make the modification because three bit symbols allow eight distinct symbols (Buternowsky: Page 6, lines 24-25).

As to claim 25, Hiratsuka discloses a data storage retrieval system that provides a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the memory device when the defective sections of the memory provide more errors than a predetermined threshold value (see claim rejection 23). Hiratsuka also discloses correcting errors in data retrieved from the memory device. Hiratsuka fails to disclose wherein the means for correcting errors comprises a single-bit per symbol error correction code.

Buternowsky discloses a communication system wherein response signals are in the form of digital packets, including forward error correction encoding and digital symbols that each consists of predetermined number of bits (Abstract, lines 3-5). Buternowsky does disclose wherein the means for correcting errors comprises a single-bit per symbol error correction code (column 6, lines 23-24).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's error correction code with Buternowsky's single-bit per symbol ECC scheme. A person of ordinary skill in the art

would have been motivated to make the modification because having a single-bit symbol would reduce the amount of noise during transmission of the error correction code (Buternowsky: Page 6, lines 24-25).

Response to Arguments

Applicant's arguments filed 8/15/2006 have been fully considered but they are not persuasive. Applicant states on page 10, "The host computer in Hiratsuka does not perform any of the error correction data error information management , or address conversion functions."

Examiner respectfully disagrees. All command information that controls disk device 100 (which is considered to be part of the host system) is inputted from the host interface (Hiratsuka: column 6, lines 40-43).

Applicant states on page 10, "The sparing system and the error correction code system recited by claim 1 are not hardware based like the disk controller disclosed by Hiratsuka."

Examiner respectfully disagrees. It is noted that the features upon which applicant relies (i.e., not hardware based) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It is noted that is obvious to one of ordinary skill in this art to implement hardware using software.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Ehne whose telephone number is (571)-272-2471. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.